REMARKS

In the Office Action, claims 1-4 and 6-9 were rejected under 35 USC §102(e) as being anticipated by Tanaka. Claims 5 and 10 were rejected under 35 USC §103(a) as being unpatentable over Tanaka in view of Pinter.

The Examiner has stated that claims 1-4 and 6-9 are rejected as being anticipated by Tanaka, i.e. U.S. Patent No. 6,600,225 (Tanaka). Like other prior art, Tanaka teaches not a method, but a semiconductor device wherein a via connection is provided in order to connect a conductive line in a lower wiring layer to conductive line in an upper wiring layer.

What evidently distinguishes Tanaka above the then prior art is the disclosure of the via being formed by two (our emphasis) conductive members formed in the space between the *upper* and lower conductive layers. This is, however, not the case with the present invention, wherein the via which discloses that the via connection proper shall be an integral part of a conductive line in the upper wiring layer, for instance a stripe electrode. Further it should be noted that the via opening of the present invention which is disclosed as having a rectangular elongate form where the longitudinal dimension is significantly greater than the transversal dimension, extends uninterrupted to an insulating layer of dielectric film provided between the electrode layers and apart

from in a preferred embodiment, having a tapered transversal side surfaces. The via opening retains its geometrical characteristics at the underlying electrode layer, i.e. by retaining its elongate form. Actually nothing is said in Tanaka of the geometry of the via opening, but an inspection of the side views in fig. 1b and 1c of Taneka et al showing the via elements 2 and 4 embedded in a dielectric film 3, shows that there can be no question of a throughgoing via opening with geometrical characteristics similar to that of the present invention.

By implication this also precludes that Tanaka in any sense anticipates the present invention with regard to a method for forming the interlayer connections or the vias of the latter. Specifically the cited passage of Tanaka relates to the geometry of the conductive elements forming the via connection by stating these to be rectangular.

Of a throughgoing via opening as disclosed in the present invention no hints or suggestions with regard to its specific form or geometrical characteristics can be found in Tanaka, apart from the fact that the volume in the dielectric layer required to accommodate the respective two conductive members of course shall differ from a conventional throughhole as evident from Tanaka, col. 5, line 64 to col. 6, line 10. As can be inferred by inspecting the drawing figures of Tanaka,

figs. 1b and 1c thereof implies that the via opening is formed in a two-step process, a first step for accommodating the conducting member 2 and extending to a height H1 with dielectric layer and a second step for accommodating the conducting member 4 and extending down to a distance H2 in the dielectric layer 3, but oriented perpendicular to the first one.

Tanaka is as stated not specifically directed to a method and anyway since the via connection is formed by two conducting elements, they cannot both be formed in the "same step as used for applying the conducting material for the conducting path on an overlying circuit layer", as stated by the Examiner. The formation of the via connection proper is a single step taking place in a single step process according to the method of the present invention, and the via connection is then formed integral with the overlying electrode or conductive line. On the contrary Tanaka states, beginning at line 7 in col. 12 that the first interlayer dielectric film 3a is deposited as shown in fig. 9a and a trench 8 formed therein and filled with a metal layer. Next follows the deposition of the second interlayer dielectric 3b and a rectangular hole 6 is formed in this second layer 3b by a conventional photomicrolithography patterning method. As evident and when a compared with figs. 1a-1c the metal of the trench 8 corresponds

to the conducting line 1 in a lower wiring layer. In a following step another interlayer dielectric film 3b is deposited over layer 3a and a rectangular hole 6 is formed in this second dielectric film 3b by conventional patterning. The surface of the lower underlying conductive line 1 is thus exposed after aligning the rectangular hole 6 and then in a following step a metal is deposited to form a metal layer filling the rectangular hole 6. A rectangular bar 2 is thus formed in this hole and forms the first conductive element 2 of the via connection as for instance shown in any of figs. 1a-1c. Now a third interlayer dielectric film 3c is deposited over the entire surface of layer 3b and conductive element 2 and a trench 9 is formed in a two-step patterning process (column 12, lines 36-38); then photolithography and etching are performed twice to form a trench 9 and a rectangular hole 7 in the interlayer dielectric film. As will be seen, the cross section of the trench 9 comprises the rectangular hole as well as a remaining step at right formed by a remaining portion 3c of the dielectric film. Now a metal film is deposited and forms a metal layer and fills both the rectangular hole and the step 9, which of course is a unitary feature 4, 5 as shown in the cross section of fig. 9c of Tanaka. Here of course both the upper conductive line and the upper conductive member is formed in

one and the same operation, but still this cannot be construed to make the method according to the present invention obvious.

The Examiner arrived at the conclusion without considering the teachings of Tanaka in greater detail by limiting the reference to the twelve lines from col. 11, line 66 to col. 12 line 6.

It is correct to say that the connecting element 4 which can be compared to a wire plug or wire is oriented parallel to the longitudinal directions of at least one stripe electrode in this case of Tanaka 5 and contained within the footprint thereof. However, this is an exact half truth because it fails to take into account that 4 is just one half of the wire connection as disclosed by Tanaka and in case of orthogonally oriented conductive lines 5 and 1 as shown in fig. 1a-1c of course only one-half of the wire connection can be contained within the footprint of a respective electrode. However, what Tanaka says in col. 5, lines 23-42 has no immediate bearing upon the via opening geometries as set forth in the present invention, but concerns the electrode dimension and dimensions of each conductive element for forming the via connection as taught by Tanaka.

The Examiner has rejected claims 5 and 10 under 35 USC 103(a) as unpatentable over Tanaka in, view of U.S. Patent No. 5,322,816 (Pinter). Pinter actually teaches a two-element

via contact with the top side contact 26 and second contact 28 on the backside of a layer of dielectric material. Similar to Tanaka or albeit structurally very different the via connection of Pinter is a two-element via connection but formed with a via opening that tapers toward the middle of a dielectric layer. It should be noted that the taper according to Pinter does not extend all the way from top to bottom of the dielectric layers 12-16 and again the via connection is formed of two separate elements and in this case they appear to be distinct from the electrodes or conducting wires in a layer comparable to that of conductive lines 1, 5 of Tanaka et al. Hence the present invention cannot be read on Tanaka in combination with Pinter as regards claims 5 and 10.

As has conclusively been proved above, the present invention is neither taught nor suggested in any sense by Tanaka or Pinter, whether taken separately or in combination. Both fail to teach the integral via connection of the present invention. Neither Tanaka nor Pinter teaches an interlayer connection that will be suitable for matrix-addressable devices of the kind as disclosed in the last section of the description of the present invention, where one commonly resorts to so-called staggered over the edge vias to form the contact between the separate electrode layers in a stacked device and

wherein one desires to reduce the real estate consumed by fan-out vias.

Finally, it should be observed that dependent claims shall be allowable in conjunction with an allowable independent claim from which they derive their dependency.

Based on the foregoing amendments and remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above amendments and remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

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